WHAT IS CLAIMED:

1. An N bit Digital-to-Analog Converter (DAC) comprising independently sized first and second current source transistors coupled to respective pluralities of first and second current provider transistors in current mirror configurations, wherein the first and second current provider transistors are sized proportionally to the first and second current source transistors respectively.

2. An N bit Digital-to-Analog Converter (DAC) comprising:

a first current provider circuit configured to provide a plurality of first current signals responsive to a plurality of first bits of an N bit data word weighted differently based on a first reference current; and

a second current provider circuit configured to provide a plurality of second current signals responsive to a plurality of second bits of the N bit data word weighted equally based on a second reference current that is different than the first reference current.

3. An N bit DAC according to Claim 2 wherein the first current provider circuit comprises a plurality of transistors of different sizes based on the first reference current.

4. An N bit DAC according to Claim 3 wherein the different sizes of the plurality of transistors are further based on respective orders of data bits of the N bit data word to which each of the respective transistors is coupled.

5. An N bit DAC according to Claim 3 wherein the first current signals have associated respective magnitudes determined based on the different sizes of the plurality of transistors

6. An N bit DAC according to Claim 3 wherein respective source/drain terminals of the plurality of transistors are coupled to the plurality of first bits.

7. An N bit DAC according to Claim 3 wherein the plurality of transistors comprises a plurality of first transistors, wherein the second current

provider circuit comprises a plurality of second transistors of about equal sizes based on the second reference current.

8. An N bit DAC according to Claim 7 further comprising:

a first current source transistor coupled to the plurality of first transistors that is configured to provide the first reference current, wherein the first current source transistor has a size about equal to a lowest order one of the plurality of first transistors; and

a second current source transistor coupled to the plurality of second transistors that is configured to provide the second reference current, wherein the second current source transistor has a size about equal to all of the plurality of second transistors.

9. An N bit DAC according to Claim 8 wherein the first and second current source transistors are sized independently of one another.

10. An N bit DAC according to Claim 7 wherein source/drain terminals of the pluralities of first and second transistors are not coupled to separate resistor components.

11. An N bit DAC according to Claim 7 wherein source/drain terminals of the pluralities of first and second transistors are each coupled to respective switches configured to switch respective bits of the N bit data word to the ones of the pluralities of first and second transistors.

12. An N bit DAC according to Claim 2 wherein the plurality of first bits comprise lower order bits of the N bit data word and the plurality of second bits comprise high order bits of the N bit data word that are higher order than the plurality of first bits, wherein the second reference current is about 2^m times as large as the first reference current, wherein m equals a lowest order one of the high order bits.

13. An N bit DAC according to Claim 2 wherein the first current provider circuit comprises a plurality of first transistors having different respective sizes relative to one another and the second current provider circuit comprises a plurality of second transistors having about equal sizes relative to one another.

14. An N bit DAC according to Claim 2 further comprising:

first and second current source transistors coupled to the first and second current provider circuits respectively; and

a current correction circuit coupled to the first and second current provider circuits and coupled to at least one of the first and second current source transistors and configured to change at least one of the first and second reference currents based on a difference between voltage levels provided by the first and second current provider circuits.

15. An N bit DAC according to Claim 14 wherein the current correction circuit is coupled to the first and second current source transistors and is configured to change the first and second reference currents based on the difference.

16. An N bit DAC according to Claim 14 wherein the current correction circuit comprises an analog-to-digital converter circuit to convert the voltage levels provided by the first and second current provider circuits to decoded digital signals representing a correction to the first or second reference current.

17. An N bit DAC according to Claim 16 further comprises:

a plurality of current correction transistors coupled to the analog-to-digital converter circuit and at least one of the first and second current source transistors and responsive to the decoded digital signals to change the first and second reference currents.

18. An N bit Digital-to-Analog Converter (DAC) comprising:

a current correction circuit configured to change at least one of first and second reference currents provided in proportion to respective sizes of transistors included in associated first and second current provider circuits based on a difference between voltage levels provided by the first and second current provider circuits.

19. An N bit DAC according to Claim 18 further comprising:

first and second current source transistors coupled to the first and second current provider circuits respectively, wherein the current correction circuit is coupled

to the first and second current source transistors and is configured to change the first and second reference currents based on the difference.

20. An N bit DAC according to Claim 18 wherein the current correction circuit comprises an analog-to-digital converter circuit to convert the voltage levels provided by the first and second current provider circuits to decoded digital signals representing a correction to the first or second reference current.

21. An N bit DAC according to Claim 20 further comprises:

a plurality of current correction transistors coupled to the analog-to-digital converter circuit and at least one of the first and second current source transistors and responsive to the decoded digital signals to change the first and second reference currents.

22. A method of operating an N bit Digital-to-Analog Converter (DAC) comprising:

providing a plurality of first current signals responsive to a plurality of first bits of an N bit data word weighted differently based on a first reference current; and

providing a plurality of second current signals responsive to a plurality of second bits of the N bit data word weighted equally based on a second reference current that is different than the first reference current.

23. A method according to Claim 22 wherein the plurality of first current signals are provided by a plurality of transistors of different sizes based on the first reference current.

24. A method according to Claim 23 wherein the different sizes of the plurality of transistors are further based respective orders of data bits of the N bit data word to which each of the respective transistors is coupled.

25. A method according to Claim 23 wherein the first current signals have associated respective magnitudes determined based on the different sizes of the plurality of transistors.

26. A method according to Claim 23 wherein respective source/drain terminals of the plurality of transistors are coupled to the plurality of first bits.

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